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ATTORNEY DOCKET NO. FILING DATE FIRST NAMED INVENTOR CONFIRMATION NO. APPLICATION NO. 02/12/2002 00100.00.0130 6702 10/074,064 Antonio Asaro EXAMINER 01/31/2006 23418 7590 **VEDDER PRICE KAUFMAN & KAMMHOLZ** MYERS, PAUL R 222 N. LASALLE STREET PAPER NUMBER **ART UNIT** CHICAGO, IL 60601 2112

DATE MAILED: 01/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary Examiner	
Paul R. Myers The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAY WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after StX (5) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 18 November 2005. 2a) This action is FINAL. 2b) This action is non-final. 3) Responsive to communication is in condition for allowance except for formal matters, prosecution as to the merical closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 1-33 is/are pending in the application.	
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5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-28,32 and 33 is/are rejected. 7) ☐ Claim(s) 29-31 is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement. Application Papers 9) ☐ The specification is objected to by the Examiner. 10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.11	21(d).
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-15.	2.
Priority under 35 U.S.C. § 119	
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.)
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4) Interview Summary (PTO-413) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152) Paper No(s)/Mail Date	

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/18/05 have been fully considered but they are not persuasive.

In regards to applicants argument that Gillespie does not teach a bridge having a ROM storing at least initial values and mask values. Initial values and Mask values are a part of configuration. The EEPROM (which is a form of ROM) stores configuration information. Gillespie also teaches Base address registers for the ASICS. Venkat teaches that initial values are part of configuration and Surugucchi teaches that Mask values for base address registers are known. Gillespie is only silent as to what is in the configuration information. Venkat and Surugucchi teach known content of configuration information.

In regards to applicants argument that the claim language of claim 28 requires a flip flop register. Gillespie teaches registers. A flip flop is a circuit that changes between two possible states. Each bit of a register has only 2 possible states, (0 and 1) and is by definition a flip flop. The examiner also notes that multi-bit registers are constructed of multiple single bit flip flops.

In regards to applicants argument that the EEPROM of Gillespie is not in the data bridge:

The data bridge is taken as items 7, 33 and 31 taken together. Also see MPEP 2144.04 V B.

In regards to applicants argument page 9-10 regarding forming the configuration from the initial values and mask values. Gillespie teaches the configuration information stored in the EEPROM 31 of the bridge being written into the configuration registers 33 of the bridge upon initialization (Column 2 lines 6-22). Venkat teaches that initial values are part of configuration and Surugucchi teaches that Mask values for base address registers are known. Thus the

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combination teaches the configuration information including the initial values and mask values are written into the configuration registers at initialization.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1, 4-11, 13, 15-17, 19, 22-23, 25-28, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083.

In regards to claims 1, 8, 10-11, 19, 28, 32: Gillespie et al teaches a data bridge system, comprising: an interface (interface to primary PCI bus 9 or alternatively interface to local memory bus 11) for transferring data; a plurality of application-specific integrated circuits (ASICs) (21 and 23); a data bridge operatively coupled to each of the interface and the plurality of ASICs (7). Gillespie et al also teaches the bridge accessing a ROM storing configuration (31 Column 1 lines 59-65). Gillespie et al does not teach and the data bridge read only memory storing at least initial values and mask values for each ASIC of the plurality of ASICS. The examiner notes Gillespie et al does teach the bridge having a plurality of Base address registers in accordance with the AGP and PCI specifications. Surugucchi et al teaches a bridge (210 or alternatively 210 and 212 taken together) including a mask register storing mask values for

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masking Base address registers in accordance with the attached peripherals. It would have been obvious to store the configuration mask values in the data bridge ROM of Gillespie et al because this would have consolidated configuration. Venkat teaches storing the initial base addresses in the configuration space of the devices. It would have been obvious to store the initial values in the configuration space of the combination of Gillespie et al in view of Surugucchi et al because this would have consolidated necessary configuration data.

In regards to claims 4, 22: Gillespie et al teaches the bridge having Base address registers. (part of the PCI specification incorporated in Gillespie)

In regards to claims 5-6, 13, 16, 23, 26: Gillespie et al teaches multiple base address registers in accordance with the PCI specification incorporated by reference in Gillespie et al.

The PCI specification notes the number of Base address registers in a bus bridge is 6.

In regards to claims 7, 15, 25: Gillespie et al teaches multiple base address registers in accordance with the PCI specification which teaches the base address registers having prefetchable and non-prefetchable and I/O space and non I/O space determinations. PCI spécification page 196.

In regards to claims 9, 17: Gillespie et al teaches a configuration EEPROM. Which is an electrically erasable programmable ROM.

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In regards to claim 27: Gillespie et al does not teach the EEPROM being removable.

MPEP 2144.04 V C states to make separable is not a patentable distinction.

4. Claims 2-3, 12, 14, 18, 20-21, 24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie et al PN 5,859,987 in view of Surugucchi et al PN 6,094,699 and Venkat PN 5,857,083 as applied to claim 1 above, and further in view of Applicants admitted prior art.

In regards to claims 2, 14, 18, 20, 24, 33: Gillespie et al does not teach the ASICs being graphics processors. Applicants admitted prior art teaches graphics processors (1020) attaches to a bus. It would have been obvious to include graphics processors because this would have allowed for the efficient control of graphics/video.

In regards to claims 3, 12, 21: Gillespie et al in view of Surugucchi et al and Venkat teach the bridge attached to a AGP bus described above. Gillespie et al in view of Surugucchi et al and Venkat do not teach a north bridge. Applicants admitted prior art teaches a north bridge attaches an AGP bus. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use the bridge of Gillespie et al in view of Surugucchi et al and Venkat in the system of Applicants admitted prior art because this would have separated the graphics from the PCI system thus freeing the PCI system.

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Allowable Subject Matter

5. Claims 29-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In regards to claims 29-31: The examiner was unable to find the exact structure claimed.

Conclusion

- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- 7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PRM January 24, 2006

PAUL FI. MYERS
PRIMARY EXAMINER

Pal R.M